TLE7279-2

Low Dropout Voltage Regulator

Automotive Power

Never stop thinking

Low Dropout Voltage Regulator **TLE7279-2**

1 Overview

Features

- Output voltage 5 V, 3.3 V
- Output voltage tolerance ±2%
- Output current up to 180 mA
- Ultra low quiescent current consumption < 36 µA
- Enable function
- Very low dropout voltage
- Reset with adjustable power-on delay
- Input Voltage Sense (Early Warning)
- Output protected against short circuit
- Wide operation range: up to 45 V
- Wide temperature range: -40 °C to 150 °C
- Overtemperature protection
- Overload protection
- Green Product (RoHS compliant)
- AEC Qualified

PG-DSO-14

Description

The TLE7279-2 is a monolithic integrated voltage regulator with early warning and reset dedicated for microcontroller supplies under harsh automotive environment conditions.

Due to its ultra low quiescent current the TLE7279-2 is perfectly suited for applications permanently connected to battery. In addition the regulator can be shut down via the Enable input causing the current consumption to drop below 3 µA. The TLE7279-2 is equipped with an output current limitation and an overtemperature shutdown protecting the device against overload, short circuit and overtemperature. It operates in the wide junction temperature range from -40 °C to 150 °C.

Type	Package	Marking
TLE7279-2GV50	PG-DSO-14	TLE7279-2GV50
TLE7279-2GV33	PG-DSO-14	TLE7279-2GV33

2 Block Diagram

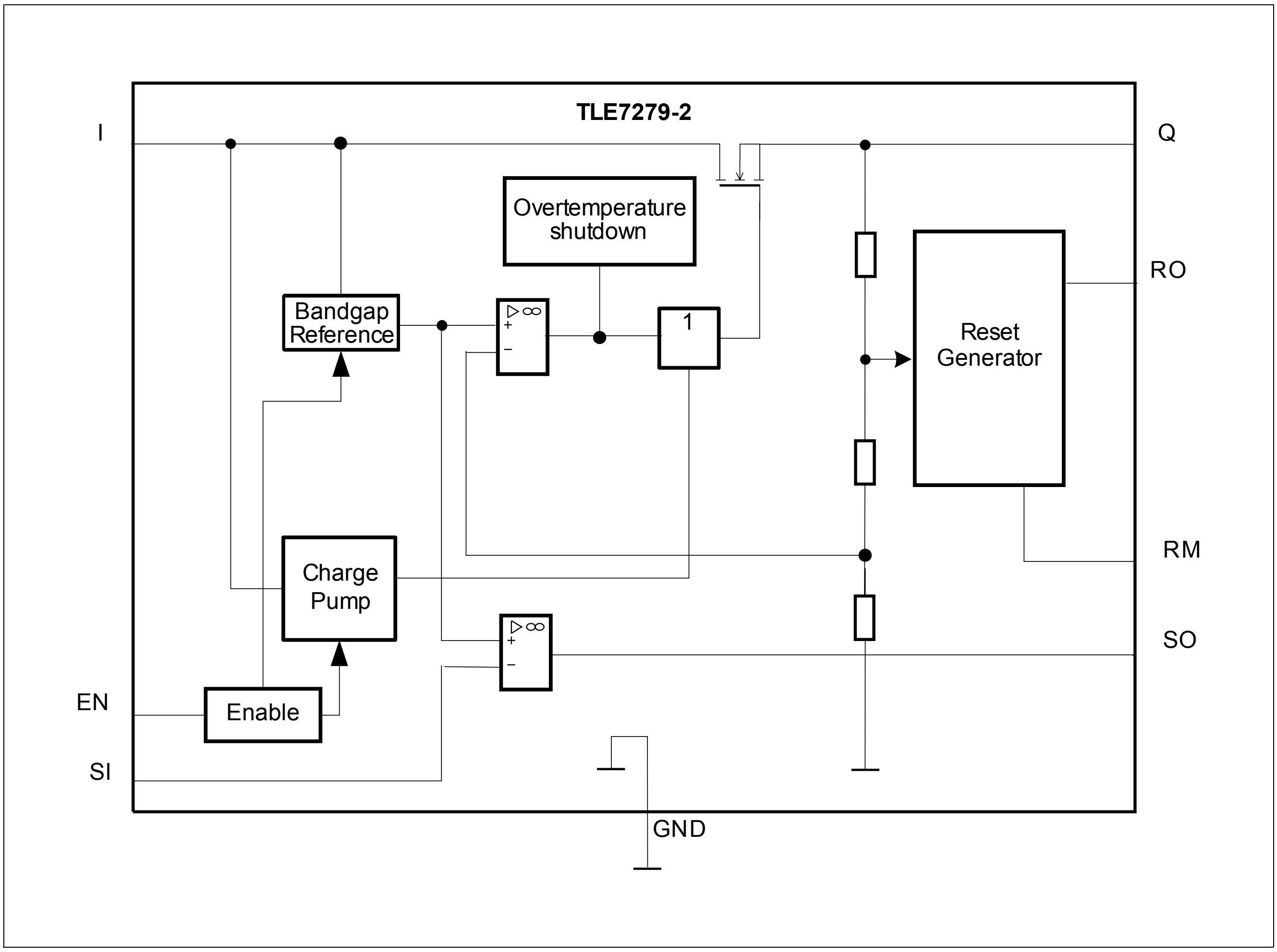


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

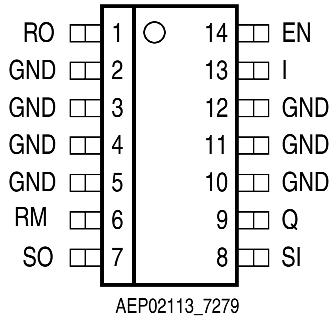


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	RO	**Reset Output** TLE7279-2GV33: open drain output; TLE7279-2GV50: integrated 20 kΩ pull-up resistor
2-5, 10-12	GND	**Ground** connect pin 2 and 3 to GND; connect pin 4-5, 10-12 to PCB heat sink area with GND potential
8	SI	**Sense Input** connect to Q if not needed
6	RM	**Reset Mode** power-on reset delay time selection: set to LOW for fast timing, to HIGH for slow timing; see reset timing definitions in **"Electrical Characteristics" on Page 9**; connect to Q or GND
7	SO	**Sense Output** TLE7279-2GV33: open-drain output; TLE7279-2GV50: integrated 20 kΩ pull-up resistor; keep open, if sense comparator not needed
9	Q	**Output Voltage** block to GND with a ceramic capacitor close to the IC terminals, respecting the values given for its capacitance and ESR in **"Functional Range" on Page 6**
13	I	**Input Voltage** block to ground directly at the IC with a 100 nF ceramic capacitor
14	EN	**Enable Input** low level disables the IC; integrated pull-down resistor to GND

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Input I, Sense Input SI						
4.1.1	Voltage	V_I, V_{SI}	-0.3	45	V	–
Output Q, Reset Output RO, Sense Out SO						
4.1.2	Voltage	V_Q, V_{RO}, V_{SO}	-0.3	5.5	V	permanent
4.1.3	Voltage	V_Q, V_{RO}, V_{SO}	-0.3	6.2	V	t < 10 s[2]
Enable Input EN						
4.1.4	Voltage	V_{EN}	-1	45	V	–
4.1.5	Current	I_{EN}	-1	1	mA	–
Reset Mode RM						
4.1.6	Voltage	V_{RM}	-0.3	5.5	V	permanent
4.1.7	Voltage	V_{RM}	-0.3	6.2	V	t < 10 s[2]
4.1.8	Current	I_{RM}	-5	5	mA	–
ESD Susceptibility						
4.1.9	Human Body Model (HBM)[3]	Voltage	–	3	kV	–
4.1.10	Charge Device Model (CDM)[4]	Voltage	–	1.5	kV	–
Temperatures						
4.1.11	Junction temperature	T_j	-40	150	°C	–
4.1.12	Storage temperature	T_{stg}	-50	150	°C	–

1) not subject to production test, specified by design
2) exposure to these absolute maximum ratings for extended periods (t > 10 s) may affect device reliability
3) ESD HBM Test according to JEDEC JESD22-A114
4) ESD CDM Test according AEC/ESDA ESD-STM5.3.1-1999

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Input voltage	V_I	5.5	45	V	TLE7279-2GV50
4.2.2			4.2	45	V	TLE7279-2GV33
4.2.3	Output capacitor's requirements for Stability	C_Q	470	–	nF	–[1]
		$ESR(C_Q)$	–	3	Ω	–[2]
4.2.4	Junction temperature	T_j	-40	150	°C	–

1) the minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

2) relevant ESR value at f = 10 kHz

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Soldering Point[1]	R_{thJSP}	–	30	–	K/W	measured to group of pins 3, 4, 5, 10, 11, 12
4.3.2	Junction to Ambient[1]	R_{thJA}	–	53	–	K/W	[2]
4.3.3			–	105	–	K/W	footprint only[3]
4.3.4			–	74	–	K/W	300 mm² heatsink area on PCB[3]
4.3.5			–	65	–	K/W	600 mm² heatsink area on PCB[3]

1) not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm³ board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 1 copper layer (1 x 70µm Cu).

5 Block Description and Electrical Characteristics

5.1 Circuit Description

5.1.1 Power On Reset and Reset Output

For an output voltage level $V_Q \geq 1$ V the reset output is hold low. When the level of V_Q reaches the reset threshold V_{RT}, the signal at RO remains low for the power-up reset delay time t_{RD}. The reset function and timing is illustrated in **Figure 3**. The reset reaction time t_{RR} avoids wrong triggering caused by short "glitches" on the V_Q-line. In case of V_Q power down ($V_Q < V_{RT}$ for $t > t_{RR}$) a logic low signal is generated at the pin RO to reset an external microcontroller.

The TLE7279-2GV50 features an integrated pull-up resistor on the reset output while the TLE7279-2GV33 have an open drain output requiring an external pull-up resistor. When connected to a voltage level of V_{ext} = 5 V, a recommended value for this external resistor is ≥ 5.6 kΩ.

But it's also possible calculating its value by using the following formula, based on the reset sink current (Example: external pull-up resistor connected to V_{ext} = 5 V):

$R_{extmin} = \Delta V / I_{RO} = (V_{ext} - V_{ROmin}) / I_{RO}$ = (5 V - 0.25 V) / 1.0 mA = 4.75 kΩ

At low output voltage levels V_Q < 1 V the integrated pull-up resistor of the TLE7279-2GV50 is switched off setting the reset output high ohmic.

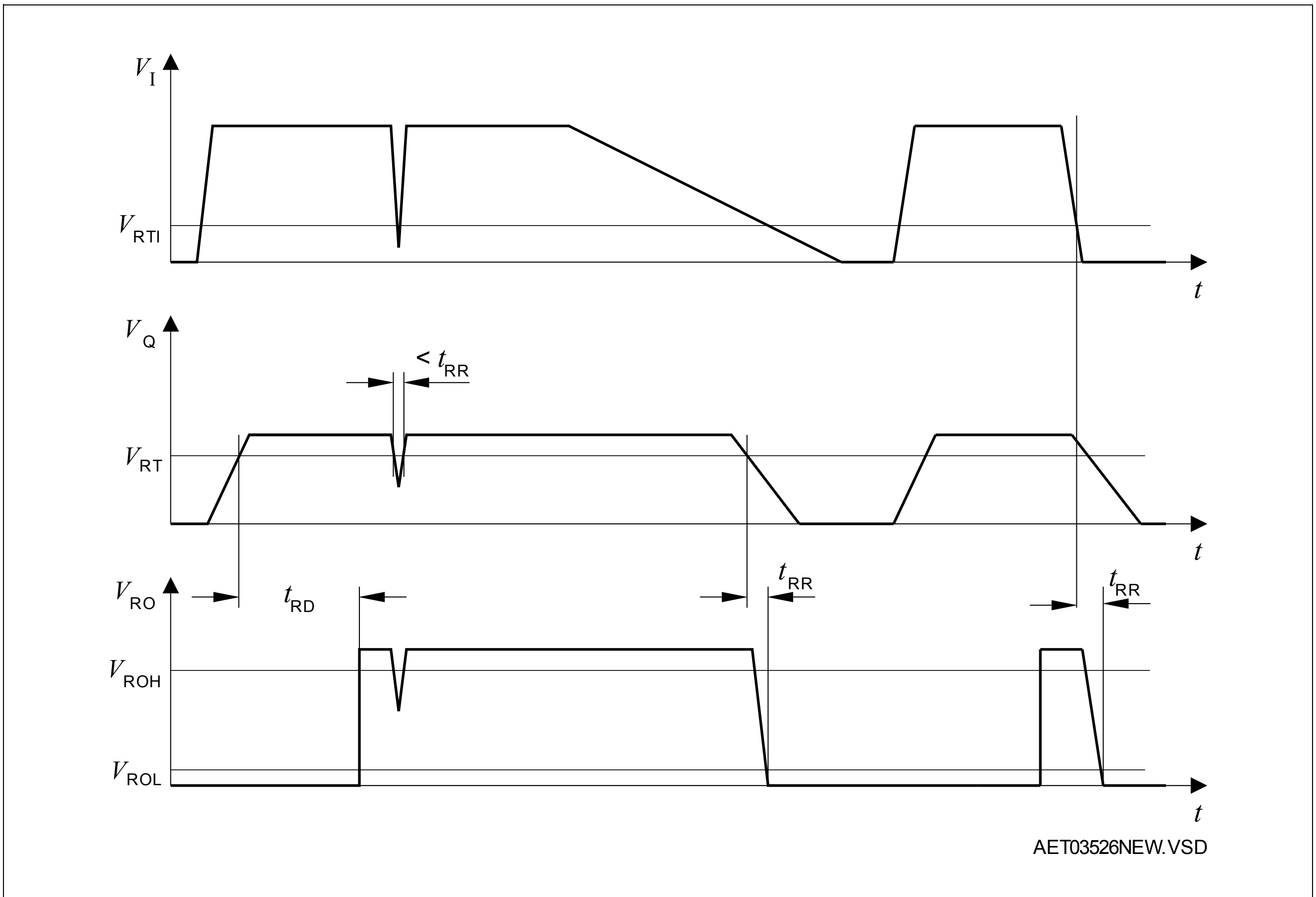


Figure 3 Reset Function and Timing Diagram

5.1.2 Early Warning

The additional sense comparator provides an early warning function: Any voltage (e.g. the input voltage) can be monitored, an undervoltage condition is indicated by setting the comparator's output to low. See **Figure 4**.

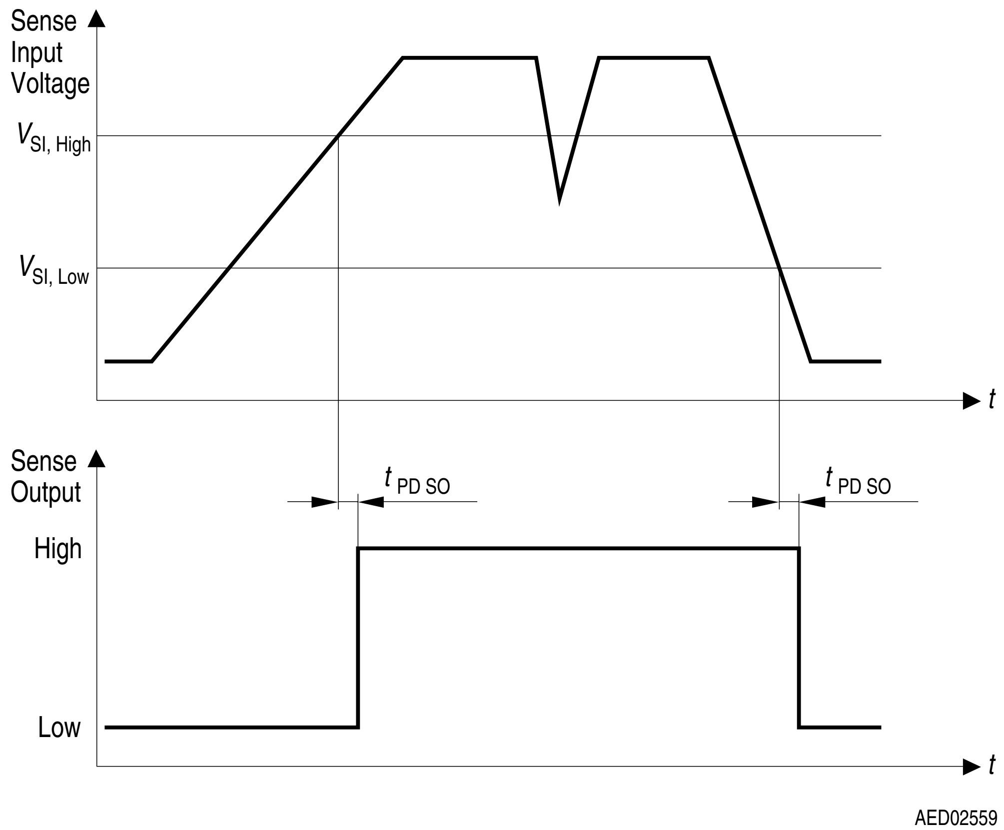


Figure 4 Early Warning Timing

The calculation of the voltage divider is easily done since the sense input current can be neglected.

$$V_{thHL} = (R_{SI1} + R_{SI2})/R_{SI2},\ V_{SI}\ \text{low} \tag{1}$$

$$V_{thLH} = (R_{SI1} + R_{SI2})/R_{SI2},\ V_{SI}\ \text{high} \tag{2}$$

The sense comparator has a hysteresis of typical 100 mV. This hysteresis of the supervised threshold is multiplied by the resistor dividers amplification $(R_{SI1} + R_{SI2})/R_{SI1}$.

The sense in comparator can also be used for receiving data with a threshold of typical 1.35 V and a hysteresis of 100 mV. Of course also the data signal can be scaled down with a resistive divider as shown above. With a typical delay time of 4 µs receiving data of up to 100 kBaud are possible.

5.2 Electrical Characteristics

Electrical Characteristics

V_I = 13.5 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Output Q							
5.2.1	Output voltage	V_Q	4.90	5.00	5.10	V	TLE7279-2GV50 1 mA < I_Q < 180 mA 6 V < V_I < 16 V
5.2.2	Output voltage	V_Q	4.90	5.00	5.10	V	TLE7279-2GV50 I_Q = 10 mA 6 V < V_I < 45 V
5.2.3	Output voltage	V_Q	3.234	3.30	3.366	V	TLE7279-2GV33 1 mA < I_Q < 180 mA 4.5 V < V_I < 16 V
5.2.4	Output voltage	V_Q	3.234	3.30	3.366	V	TLE7279-2GV33 I_Q = 10 mA 4.5 V < V_I < 45 V
5.2.5	Output current limitation	I_Q	200	–	500	mA	V_Q = 2.0 V
			200	–	600	mA	V_Q = 0 V
5.2.6	Dropout voltage; $V_{DR} = V_I - V_Q$	V_{DR}	–	250	500	mV	I_Q = 180 mA[1)]
5.2.7	Load regulation	$\Delta V_{Q,Lo}$	–	50	90	mV	1 mA < I_Q < 180 mA
5.2.8	Line regulation	$\Delta V_{Q,Li}$	–	10	50	mV	I_Q = 1 mA; 10 V < V_I < 32 V
5.2.9	Power-Supply-Ripple-Rejection	$PSRR$	–	60	–	dB	f_r = 100 Hz; V_r = 0.5 Vpp
5.2.10	Reverse Output Current Clamping	$V_{Q,REV}$	–	–	5.5	V	$I_{Q,REV}$ = -1 mA; V_{EN} = 0 V
Current Consumption							
5.2.11	Quiescent current; $I_q = I_I - I_Q$	I_q	–	28	36	µA	I_Q = 100 µA; T_j < 80 °C
5.2.12	Quiescent current; Disabled	I_q	–	1	3	µA	V_{EN} = 0 V; T_j < 80 °C
Enable Input EN							
5.2.13	High Level Input Voltage	$V_{EN,H}$	3.0	–	–	V	V_Q on
5.2.14	Low Level Input Voltage	$V_{EN,L}$	–	–	0.5	V	V_Q = 0.02 V I_Q = 5 mA T_j < 125 °C
5.2.15			–	–	0.3	V	V_Q = 0.02 V I_Q = 5 mA
5.2.16	High Level Input current	$I_{EN,H}$	–	3	4	µA	V_{EN} = 5 V

Electrical Characteristics (cont'd)

V_I = 13.5 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Reset Mode Bit RM							
5.2.17	High Level Input Voltage	$V_{RM,H}$	4.00	–	–	V	TLE7279-2GV50
5.2.18			2.65	–	–	V	TLE7279-2GV33
5.2.19	Low Level Input Voltage	$V_{RM,L}$	–	–	0.80	V	–
Input Voltage Sense							
5.2.20	Sense threshold high	V_{SIH}	1.10	1.16	1.22	V	V_{SI} increasing (see Figure 3)
5.2.21	Sense threshold low	V_{SIL}	1.06	1.12	1.18	V	V_{SI} decreasing (see Figure 3)
5.2.22	Sense input switching hysteresis	$V_{SI\ HYST}$	25	–	75	mV	$V_{SI\ HYST} = V_{SIH} - V_{SIL}$
5.2.23	Sense output low current	I_{SOL}	–	–	1.1	mA	V_{SI} < 1.01 V; V_I > 4.2 V; EN = High; V_{SOL} < 0.4 V
5.2.24	Sense output low voltage	V_{SO}	–	0.15	0.25	V	V_{SI} < 1.01 V; V_I > 4.2 V; EN = High; I_{SO} < 200 µA
5.2.25	Sense high voltage	V_{SOH}	4.5	–	–	V	TLE7279-2GV50
5.2.26	Sense high leakage current	I_{SOLK}	–	–	1	µA	TLE7279-2GV33
5.2.27	Integrated sense pull-up resistor	R_{SO}	10	20	40	kΩ	TLE7279-2GV50 internally connected to V_Q
5.2.28	Sense input current	I_{SI}	-1	0.1	1	µA	V_{SI} = 5 V
5.2.29	Sense reaction time	$t_{pd\ SO}$	–	4.0	–	µs	–
Reset Output RO							
5.2.30	Output Undervoltage Reset Switching Threshold	V_{RT}	4.50	4.60	4.70	V	TLE7279-2GV50 V_Q decreasing
5.2.31			3.00	3.07	3.13	V	TLE7279-2GV33[2)] V_Q decreasing
5.2.32	Input Voltage Reset Switching Threshold	V_{RT_VI}	–	3.9	4.0	V	TLE7279-2GV33[2)] V_Q > V_{RT}, V_I decreasing
5.2.33	Reset Hysteresis	V_{RH}	–	60	–	mV	TLE7279-2GV33
5.2.34			–	90	–	mV	TLE7279-2GV50
5.2.35	Maximum Reset Sink Current	$I_{RO,max}$	1.75	–	–	mA	TLE7279-2GV50 V_Q = 4.5 V, V_{RO} = 0.25 V
5.2.36			1.3	–	–	mA	TLE7279-2GV33 V_Q = 3.0 V, V_{RO} = 0.25 V
5.2.37	Reset output low voltage	V_{ROL}	–	0.15	0.25	V	$V_Q \geq$ 1 V; I_{RO} < 200 µA

Electrical Characteristics (cont'd)

V_I = 13.5 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.2.38	Reset high voltage	V_{ROH}	4.5	–	–	V	TLE7279-2GV50
5.2.39	Reset high leakage current	I_{ROLK}	–	–	1	µA	TLE7279-2GV33
5.2.40	Integrated reset pull-up resistor	R_{RO}	10	20	40	kΩ	TLE7279-2GV50 internally connected to V_Q
5.2.41	Power-on reset delay time	T_{RD}	12.8	16.0	19.2	ms	fast reset timing RM = Low
			25.6	32.0	38.4	ms	slow reset timing RM = High
5.2.42	Reset Reaction Time	T_{RR}	–	4	12	µs	–[3)

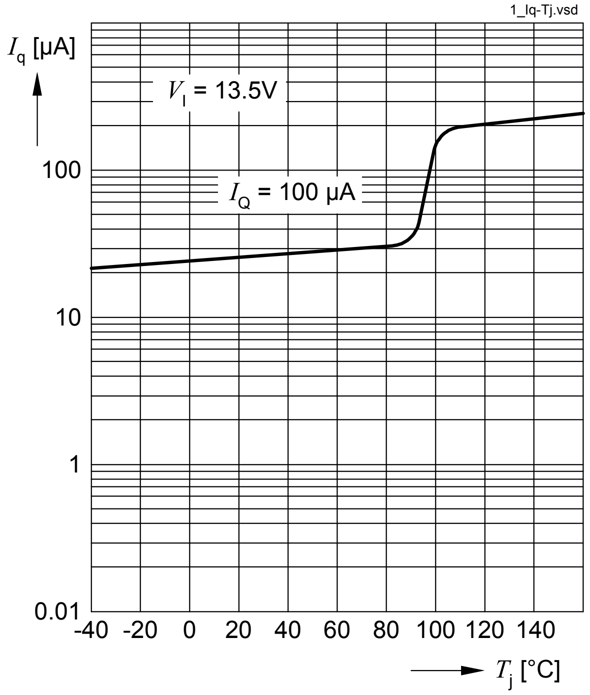
1) measured when the output voltage has dropped 100 mV from the nominal value obtained at V_I = 13.5 V

2) reset output triggered when output voltage V_Q is lower than output voltage reset switching threshold V_{RT} or is also triggered, when Input Voltage is decreasing to V_I < 4.0 V and V_Q > V_{RT}

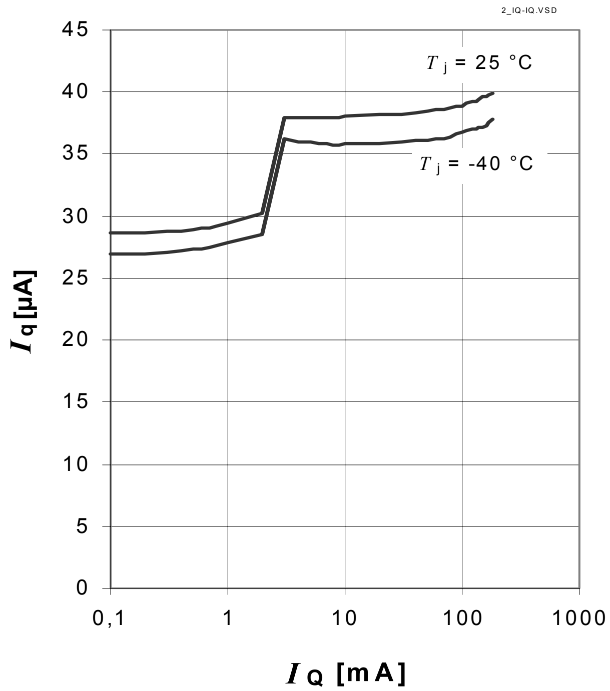
3) not subject to production test, specified by design

Typical Performance Characteristics

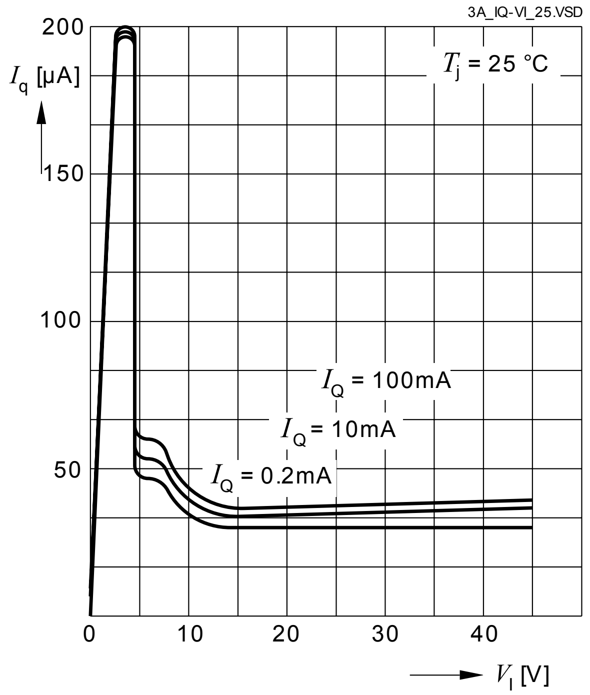
Current Consumption I_q versus Junction Temperature T_j (EN=ON)



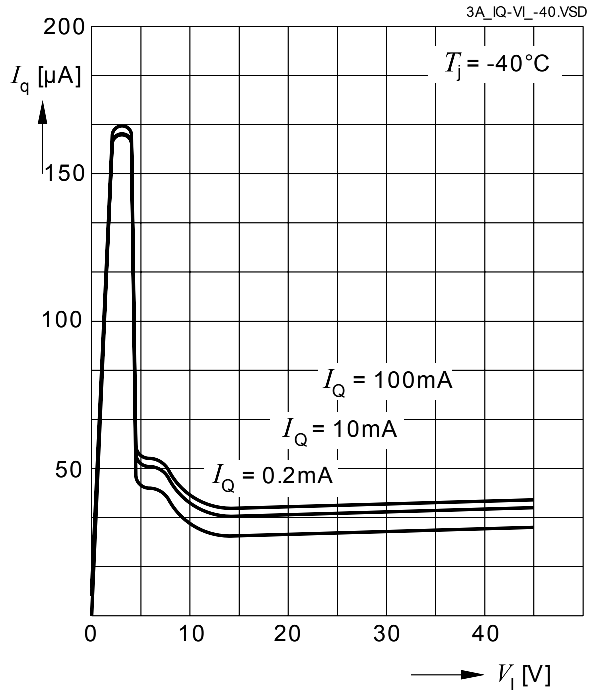
Current Consumption I_q versus Output Current I_Q (EN=ON)



Current Consumption I_q versus Input Voltage V_I at T_j=25°C (EN=ON)

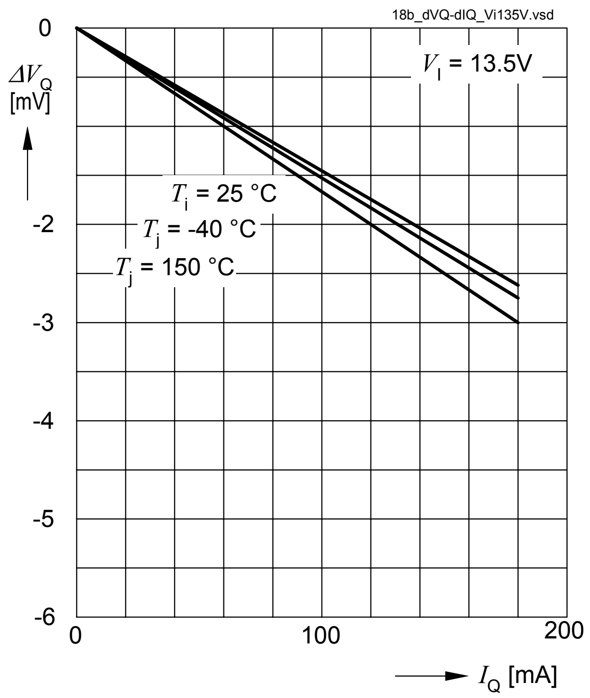


Current Consumption I_q versus Input Voltage V_I at T_j=-40°C (EN=ON)

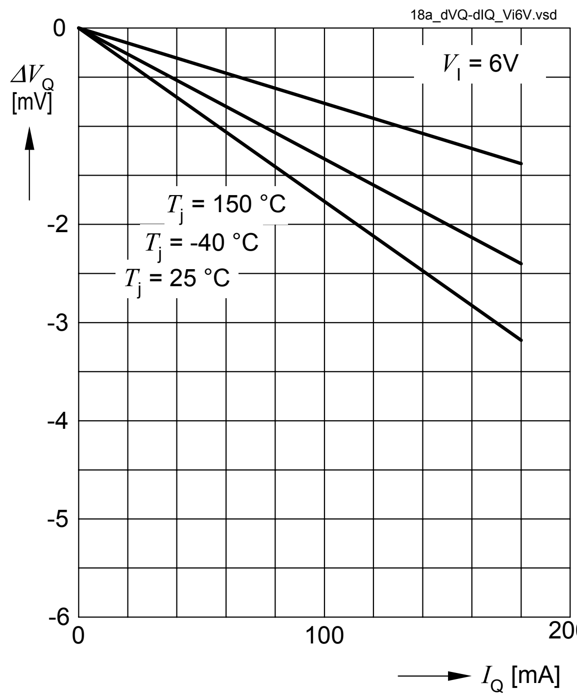


Typical Performance Characteristics (cont´d)

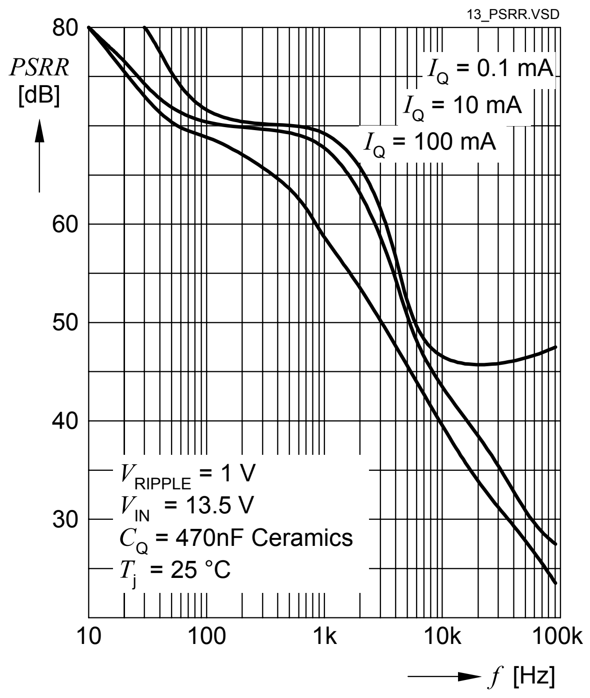
Load Regulation dV_Q versus Output Current Change dI_Q



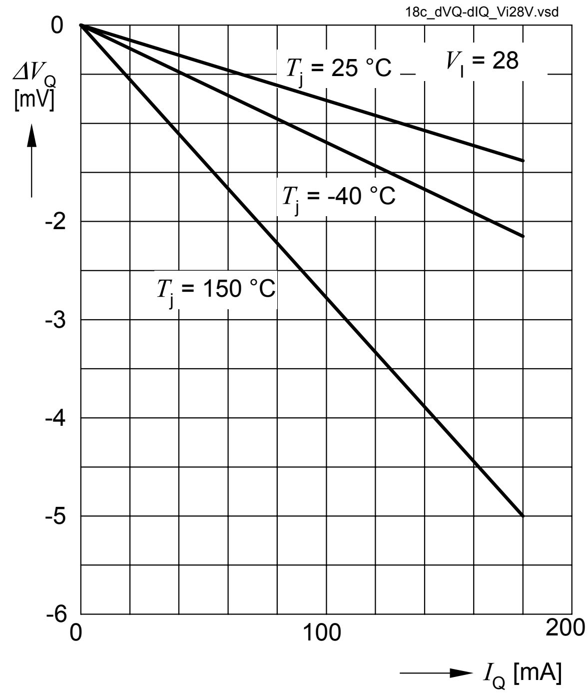
Load Regulation dV_Q versus Output Current Change dI_Q



Power Supply Ripple Rejection *PSRR*

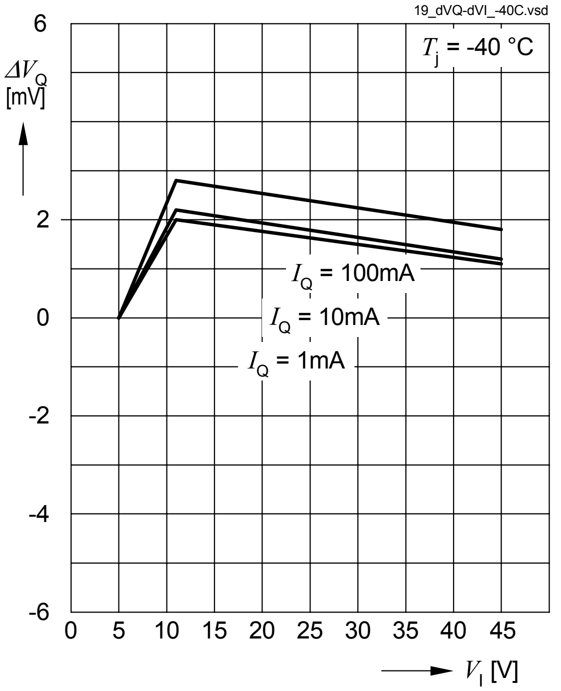


Load Regulation dV_Q versus Output Current Change dI_Q

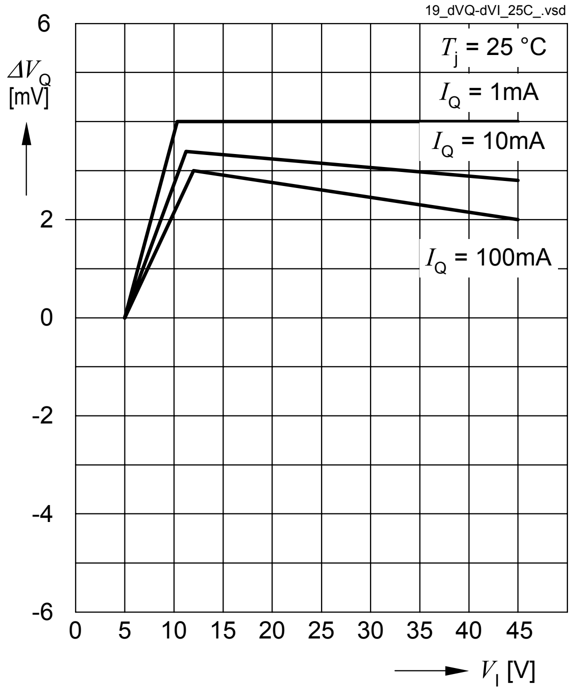


Typical Performance Characteristics (cont´d)

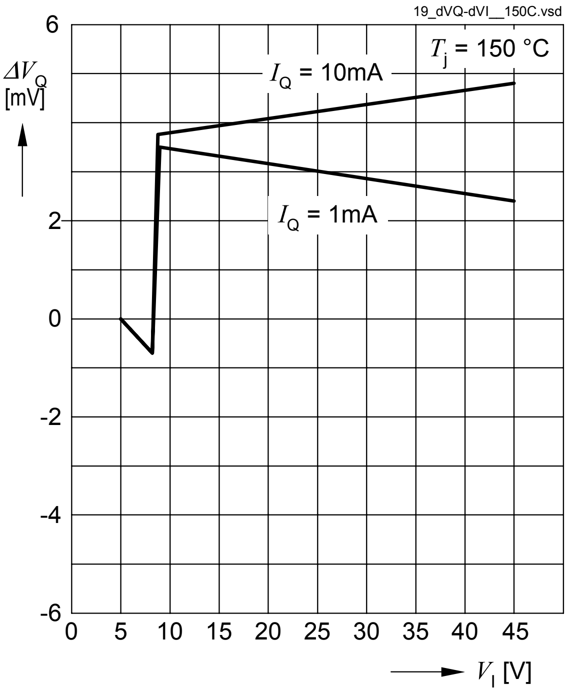
Line Regulation dV_Q versus Input Voltage Change dV_I



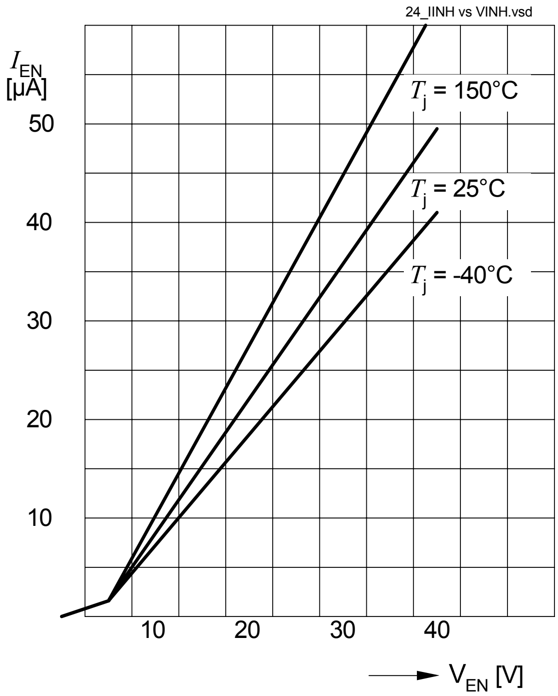
Line Regulation dV_Q versus Input Voltage Change dV_I



Line Regulation dV_Q versus Input Voltage Change dV_I

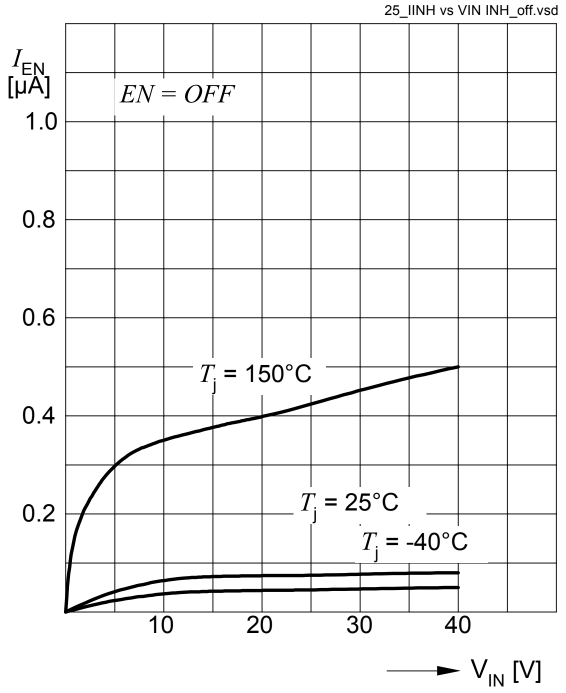


Enable Input Current I_{EN} versus Enable Input Voltage V_{EN}

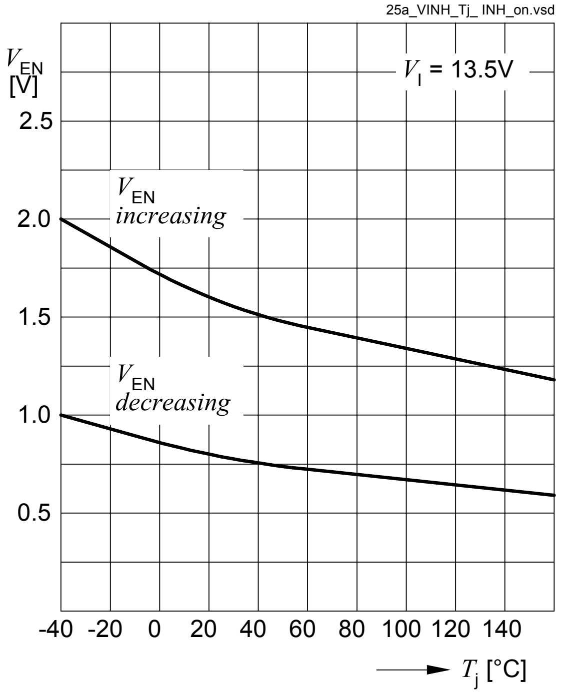


Typical Performance Characteristics (cont´d)

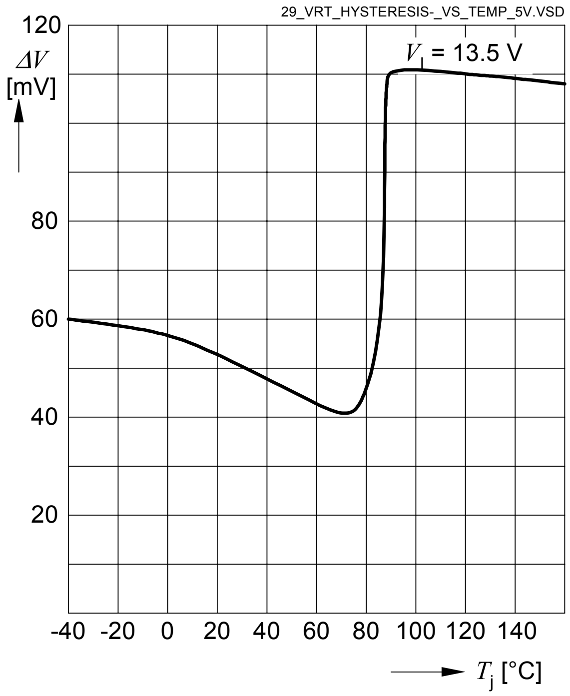
Enable Input Current I_{EN} versus Input Voltage V_I, EN=Off



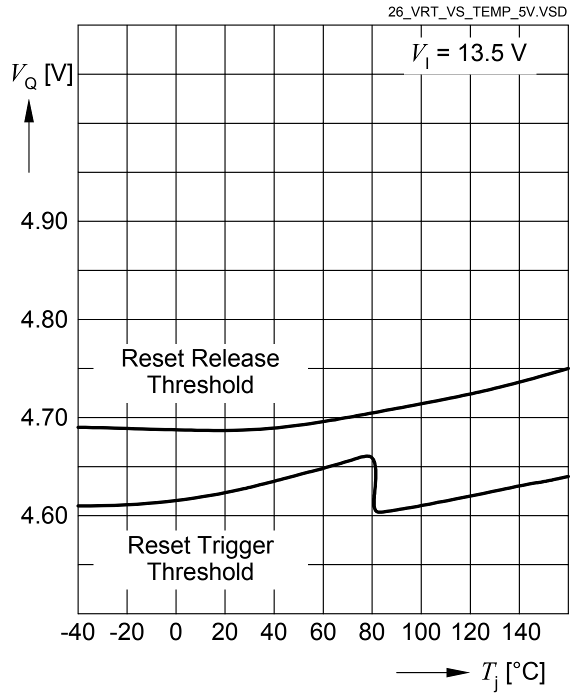
Enable High Level / Low Level Input Voltage $V_{EN,H}$ / $V_{EN,L}$ versus Junction Temperature T_j



Reset Hysteresis versus Junction Temperature T_j (5V-Version)

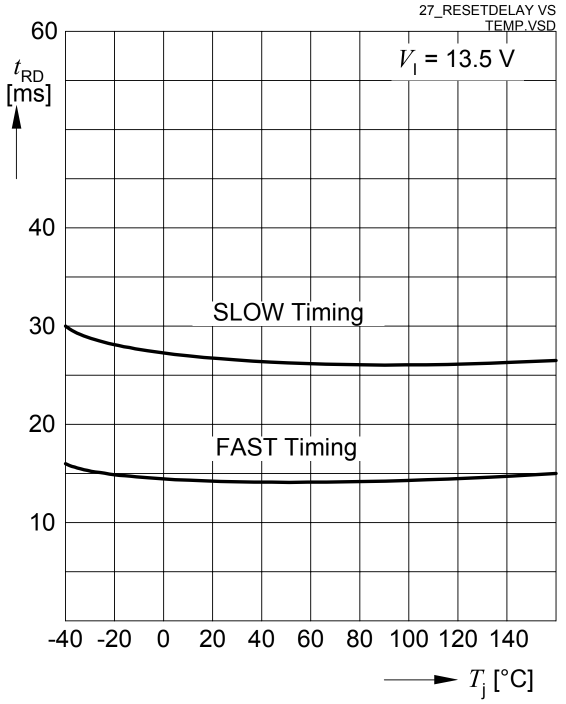


Reset Threshold V_{RT} versus Junction Temperature T_j (5V-Version)

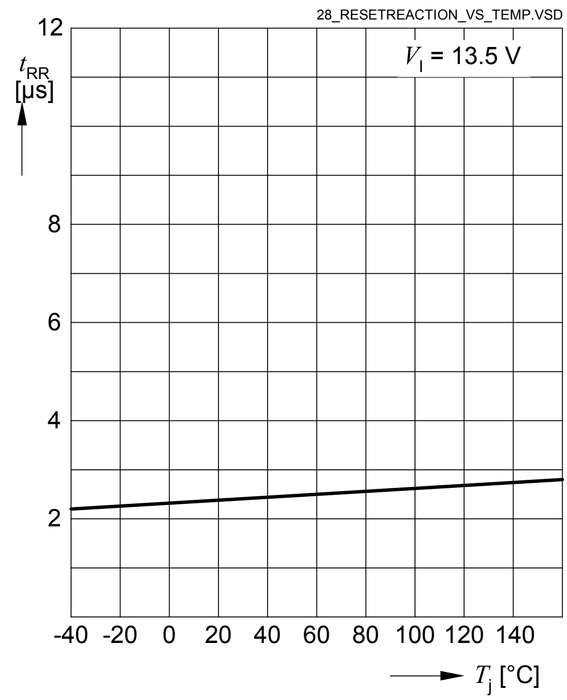


Typical Performance Characteristics (cont´d)

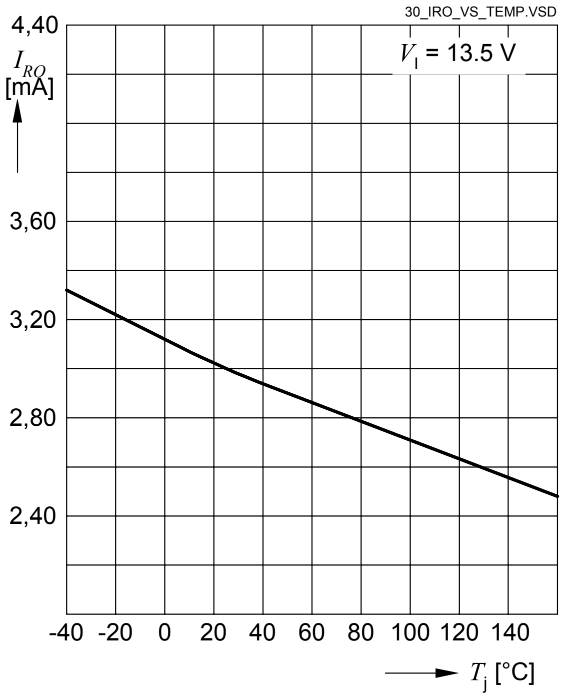
Reset Delay t_{RD} Time versus Junction Temperature T_j



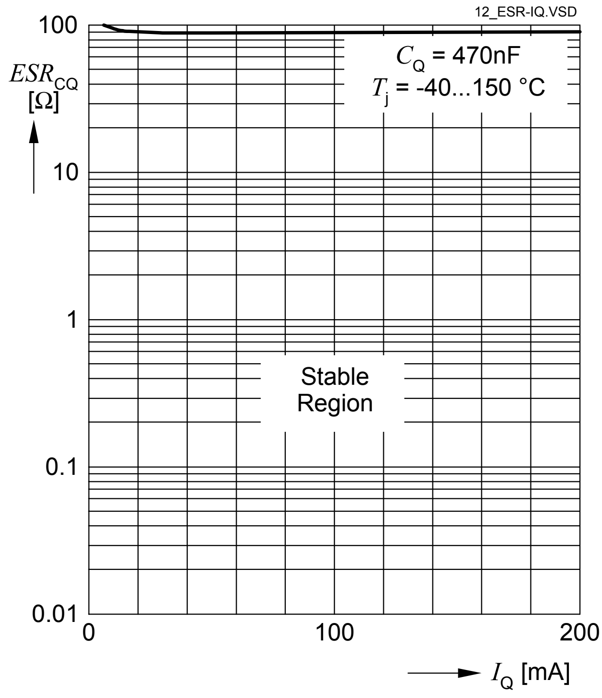
Reset Reaction Time t_{rr} versus Junction Temperature T_j



Reset Output Sink Current I_{RO} versus Junction Temperature T_j



Region of Stability $ESR(C_Q)$ versus Output Current I_Q



6 Package Outlines

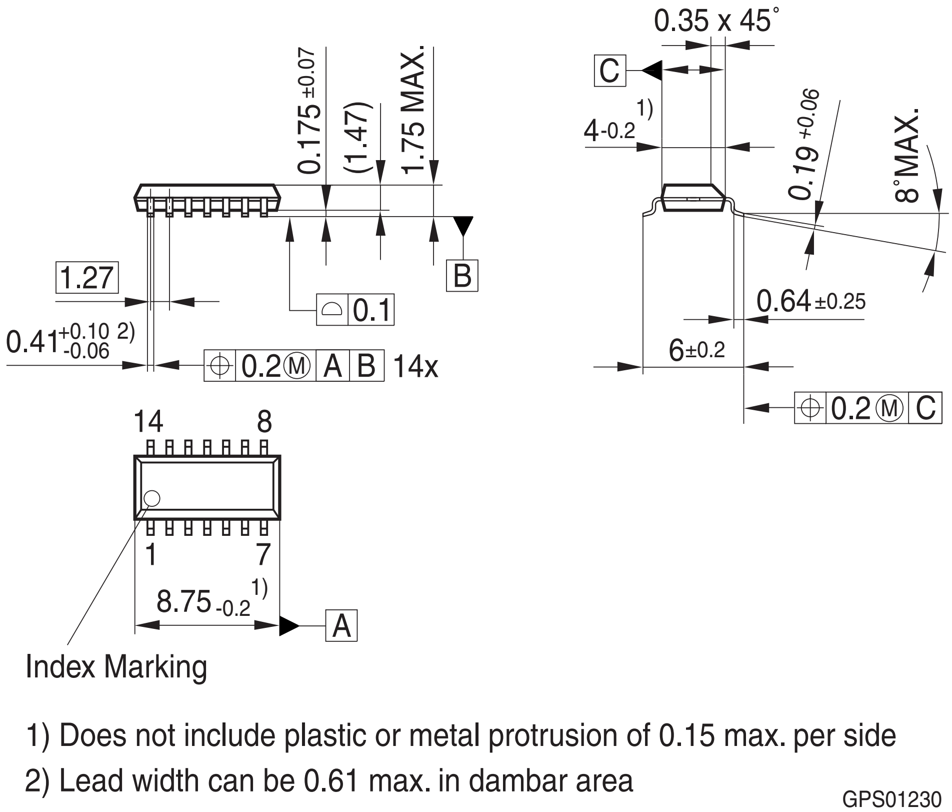


Figure 5 **PG-DSO-14** (Plastic/Plastic Green - Dual Small Outline Package)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

7 Revision History

Revision	Date	Changes
1.1	2008-07-25	3.3V version and all related description added:
		In **“Features” on Page 2**“ 3.3V” added
		In **“Overview” on Page 2** in table at the bottom type “TLE7273-2GV33” added
		In **“Pin Definitions and Functions” on Page 4** in description for Pin 1 and Pin 7 “TLE7273-2GV33: open drain output;” added
		In **“Functional Range” on Page 6 Item 4.2.2** added
		In **“Power On Reset and Reset Output” on Page 7** description for dimensioning external pull-up resistor at RO added
		In **“Electrical Characteristics” on Page 9** all specific Items for 3.3V version added: **Item 5.2.3**, **Item 5.2.4**, **Item 5.2.18**, **Item 5.2.26**, **Item 5.2.31**, **Item 5.2.32**, **Item 5.2.33**, **Item 5.2.36** and **Item 5.2.39** added
1.0	2008-04-10	final version data sheet

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